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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/644,718 | 08/20/2003 | Yi-Hsun Wu | N1085-00191 | 6119 |

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| EXAMINER | |
|---|---|
| NGUYEN, DANNY | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

A

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/644,718 | WU ET AL. | |
| | Examiner | Art Unit | |
| | Danny Nguyen | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The specification describes a voltage divider includes plural of series diodes. How is the series diodes (251) formed a voltage divider?

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10, 13-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Dungan et al (USPN 5,311,391).

Regarding claim 1, Dungan discloses a sensor (51 and 57) for electrostatic discharge protection comprises a voltage divider (series diodes 51a-51e) coupled to an input terminal (17) of the sensor, wherein a voltage drop occurs across the voltage divider and a high state voltage is generated at an output terminal (53) of the sensor when the input terminal of the sensor is coupled to an ESD voltage pulse (ESD voltage pulse on terminal 17), and a device (such as 51f) coupled to the voltage divider, wherein

the device is adapted to maintain the high state voltage at the output terminal of the sensor, while the input terminal of the sensor is coupled to the ESD voltage pulse (e.g. col. 4, lines 5-67).

Regarding claims 2, 16, Dungan discloses the input terminal of the sensor is coupled to a voltage supply terminal (13).

Regarding claims 3, 4, 17, 18, Dungan discloses the voltage divider is a series of diodes (51a-51e).

Regarding claims 5-7, 19-21, Dungan discloses the device is NMOS transistor (e.g. 51f), which has a gate terminal, and a drain terminal is common.

Regarding claims 8-10, Dungan discloses the output terminal of the sensor is coupled to an inverter (65), and the inverter is coupled to an ESD circuit (47).

Regarding claim 13, Dungan discloses a circuit (figure 2) for ESD protection comprises an ESD circuit (45) having a MOS transistor (47) with a gate terminal, a sensor (51) that senses an ESD pulse and generates a high state voltage at an output terminal (55) in response to the ESD pulse, and an inverter (65) coupled to the output terminal and the ESD circuit.

Regarding claim 15, Dungan discloses a sensor (51) for electrostatic discharge protection comprises a voltage divider (series diodes 51a-51e) coupled to an input terminal (17) of the sensor, wherein a voltage drop occurs across the voltage divider and a high state voltage is generated at an output terminal (53) of the sensor when the input terminal of the sensor is coupled to an ESD voltage pulse (ESD voltage pulse on terminal 17), and a device (such as 51f) coupled to the voltage divider, wherein the

device is adapted to maintain the high state voltage at the output terminal of the sensor, while the input terminal of the sensor is coupled to the ESD voltage pulse (e.g. col. 4, lines 5-67).

3. Claims 1, 8-10, 13, 14, 23-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Yu (USPN 6,014,298).

Regarding claims 1, Dungan discloses a sensor (R2, C2, 32) for electrostatic discharge protection comprises a voltage divider (series diodes R2, C2) coupled to an input terminal of the sensor, wherein a voltage drop occurs across the voltage divider and a high state voltage is generated at an output terminal of the sensor when the input terminal of the sensor is coupled to an ESD voltage pulse, and a device (such as 30) coupled to the voltage divider, wherein the device is adapted to maintain the high state voltage at the output terminal of the sensor, while the input terminal of the sensor is coupled to the ESD voltage pulse (col. 3, 4, lines 51-7).

Regarding claims 8-10, Yu discloses the output of the sensor is connected to an inverter (30), the inverter is coupled to an ESD circuit (M2).

Regarding claims 13, 14, Yu discloses a circuit (figures 2, 4) for ESD protection comprises an ESD circuit (28) having a MOS transistor (M1) with a gate terminal, a sensor (R2, C2, 32) that senses an ESD pulse and generates a high state voltage at an output terminal (high state generated at the output terminal of the inverter 32) in response to the ESD pulse, and an inverter (30) coupled to the output terminal and the ESD circuit (col. 3, 4, lines 51-7).

Regarding claims 23, 24, Yu discloses a method for ESD protection comprises sensing an ESD pulse (the ESD pulse is sensed by the RC detection circuit and 32, see figure 4), pulling down a gate terminal of a MOS transistor (M2) of an ESD circuit (28) to a low state when the ESD pulse is sensed (col. 3, 4, lines 51-7).

Regarding claims 25, 26 Yu discloses connecting the sensor to a voltage supply terminal (Vdd) and generating a high state voltage at the output terminal when the ESD pulse is sensed.

Regarding claims 27, 28 Yu discloses the output terminal of the sensor is coupled to an inverter (30) to generate a low state at an output terminal of the inverter when the ESD pulse is sensed (col. 3, 4, lines 51-7).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11, 12, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Smith et al (USPN 6,775,112).

Regarding claims 11, 22, Yu discloses all limitations of claim 1 as discussed above, but, Yu does not disclose the cascaded transistor as claimed. Smith discloses an ESD circuit comprises a MOS transistor of ESD circuit is cascaded NMOS (300) (figures 3 and 4). It would have been obvious to one of ordinary skill in the art at the

time the invention was made to have modified the circuit of Yu to incorporate the cascaded transistor as disclosed by Smith in order to provide efficient ESD protection.

Regarding claim 12, Yu discloses the gate of the MOS transistor (M2) is pulled down to a low state when the ESD pulse is sensed (col. 3, 4, lines 51-7).

***Conclusion***

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (571)-272-2054. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DN
10/24/2006

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